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Performance Evaluation of a Three Phase Nine Level Inverter with Reduced Switch Count

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Abstract: This paper presents a three phase nine level cascaded H-bridge (CHB) multilevel inverter with RL load. A sinusoidal and trapezoidal PWM method is used to achieve minimum total harmonics distortion (THD) in the output current of multilevel inverters. The analysis of the output current harmonics is carried out and compared with the seven level conventional cascaded H-bridge inverters. The proposed inverter is verified through simulation and the simulation results are compared with the conventional multilevel inverter. From the result the proposed inverter offers much less total harmonic distortion.

Keywords: THD; CHB; Three phase inverter.

1. Introduction

Multilevel inverter topology has gained much attention in recent years due to their various advantages. The general techniques of multilevel inverters involve the applying a higher number of power semiconductor switches to perform the power conversion in minimum voltage steps. The minimum voltage steps lead to obtain the switching losses and low harmonic distortion, devices possessing high efficiency and low voltage ratings. Al-Judi and Nowicki [1] to depreciate the electromagnetic interference effects and also reduce the output distortion. Dordevic, *et al.* [2] the ratio of the switching frequency to fundamental frequency is high. Derivation is based on the integrations of the power of the Pulse width modulation signal in a single switching period above the fundamental period of the signal. Only sinusoidal reference voltages are examined and no injection of any method is considered. Fengjiang, *et al.* [3] to apply the same comparison logics of the modulation waves and carrier during positive and negative half cycles of the MWs. Thus, it is applied with only one digital signal processor chip without any other attached logical controller. Ghazanfari, *et al.* [4] the cascaded H-bridge configuration of multilevel inverters is widely used because of its ability to generate near sine output waveforms, simple circuit, modular structure and high reliability. Junfeng and Yuanmao [5] the output harmonic order and the component counter can be significantly decreased by the maximum number of voltage levels. Liming, *et al.* [6] a power-distribution technique among the energy source, the segmented energy storage, and electric motor is proposed under various operation modes. Rahim, *et al.* [7] three reference output signals that are identical to each other with an offset that is equivalent to the amplitude of the triangular carrier output signal were used to generate the PWM signals. Ronny, *et al.* [8] in this topology, the output Switching frequency is double the filter ripple frequency, therefore reducing the magnetic weight and volume. Samuel, *et al.* [9] the cascaded H-bridge inverter has been used as a Voltage source inverter and operated in a current control mode in order to attain the objectives of real power injection and load compensation based on the proposed reference-generation method. Yousedfpoor, *et al.* [10] multilevel inverters with a fundamental frequency switching technique, the switching angles can be selected so that the output THD is reduced.

2. Proposed Nine Level Inverter

The proposed symmetrical nine level inverter comprised of four dc voltage (V1, V2, V3, V4) sources and seven power semiconductor switches(S1, S2, S3, S4, S5, S7, S8) with RL(Resistive and Inductive) load. The inverter can generate Nine different voltage outputs: +4Vdc, +3Vdc ,+2Vdc, +Vdc, 0, -Vdc, -2Vdc, -3Vdc, -4Vdc. As the very important part in multilevel inverters are switches which define the reliability, cost, circuit size and installation area.

The number of required power switches versus required voltage levels is the most important element in the design. To provide a maximum number of output levels without increasing the number of H-bridges, a new power

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circuit topology and a suitable method to determine the current source level for symmetrical multilevel inverter are proposed. The proposed inverter also provides reduced voltage stress on the switch by the series configuration of the utilized bidirectional switches. This subsequently increases the immunity from overvoltage and dv/dt breakdown. Fig .1 shows a configuration of the proposed symmetrical 9- level inverter. In case of table.1, it generate 9-level output.

Figure-1. Proposed three-phase 9- level inverter

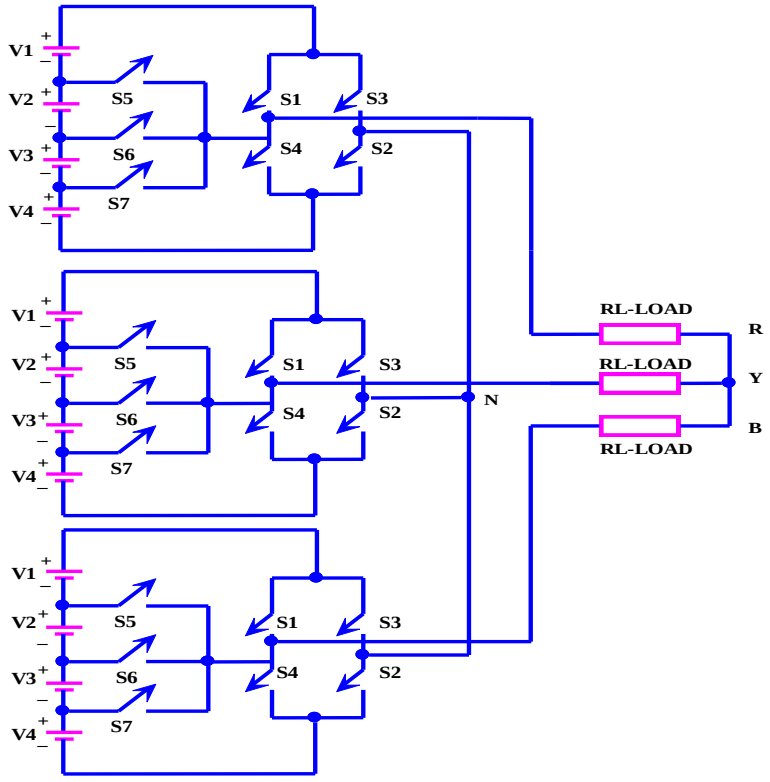


Table-1. Proposed three phase 9-level inverter

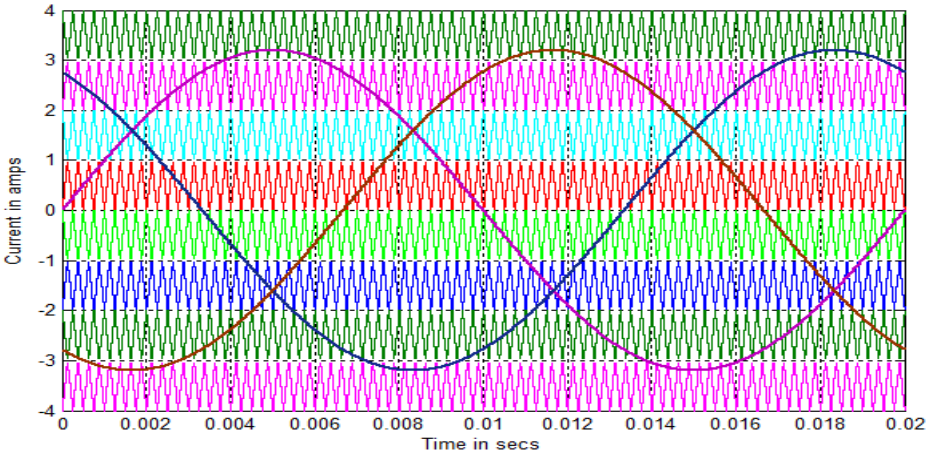
S_1	S_2	S_3	S_4	S_5	S_6	S_7	OUTPUT VOLTAGE
1	1	0	0	0	0	0	$4V_{dc}$
1	1	0	0	1	1	0	$3V_{dc}$
1	1	0	0	1	0	1	$2V_{dc}$
1	1	0	1	1	0	0	V_{dc}
1	0	1	0	0	0	0	0
0	0	1	0	0	1	1	$-V_{dc}$
0	0	1	1	0	1	0	$-2V_{dc}$
0	0	1	1	0	0	1	$-3V_{dc}$
0	0	1	1	1	1	1	$-4V_{dc}$

3. Modulation Technique

Several modulation techniques have been developed for multilevel inverters. The most common method used is the multi carrier sub harmonic PWM technique. The principle of the multicarrier PWM technique is based on a comparison of a sinusoidal and trapezoidal reference waveform with triangular carrier waveforms. m-1 carriers are needed to generate m levels. The carrier waves are in continuous bands around the reference zero. They have the same frequency fc and the same amplitude Ac. The sinusoidal and trapezoidal reference waveform has a frequency fr and Ar is the peak to peak value of the reference waves. At each instant, the result of the comparison is one if the triangular carrier waves are greater than the reference signal and zero otherwise. The output of the modulator is the sum of the various comparisons which represents the current level.

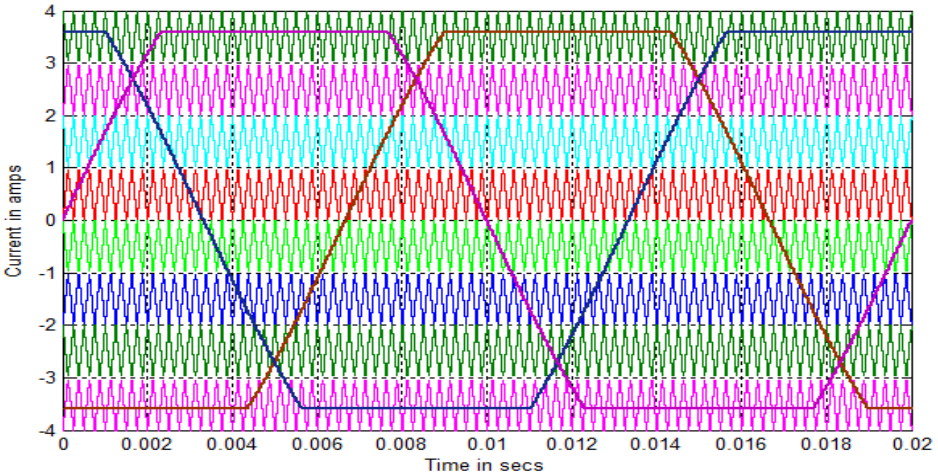
Eight triangular signals presents in the proposed nine-level inverter is 180 degree out of phase with each other. So it is called as APODPWM (Alternate Phase Opposition & Disposition Pulse Width Modulation) control technique.

Figure-2. Carrier arrangements for APODPWM technique with sinusoidal reference



This trapezoidal reference is almost similar to sinusoidal reference with APODPWM technique. Figure 3 shows the carrier arrangement for APODPWM method for m_a = 0.9 and m_f =40.

Figure-3. Carrier arrangements for APODPWM technique with trapezoidal reference



4. Simulation Results

Simulation of proposed three phase symmetrical nine level inverter with RL load is carried out by MATLAB/ SIMULINK. Switching signals for Cascaded Multi Level Inverter (CMLI) are developed using PWM techniques but for only one sample technique are used for the both references. The simulation results are performed for various modulation indices (ma=0.6-1) and for all the PWM techniques. The corresponding % THD values and IRMS of fundamental and peak amplitude current IPEAK of inverter output for same modulation indices corresponding of FFT plots and they are shown in tables 2-7.Figures shows the simulated output current waveform for a CMLI and corresponding FFT plots for sinusoidal reference chosen the one sample value of ma = 0.8 and for trapezoidal reference chosen the one sample value of ma = 0.9. Tables 2 – 7 obtain the performance measures such as %THD, IRMS and IPEAK. Figures 4 – 22 shows the three-phase output current waveforms for sinusoidal and trapezoidal references and its respective FFT plots.

Figure-4.1. Three-phase output current waveform for PDPWM technique with sinusoidal reference

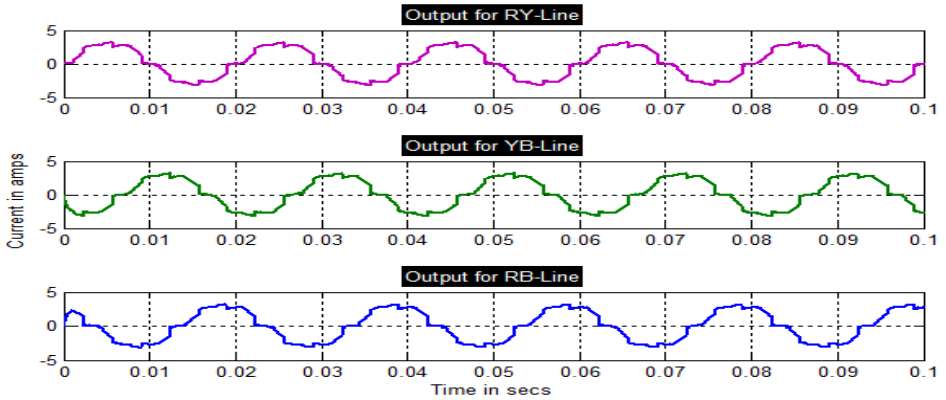


Figure-4.2. FFT Plot for output current Of PDPWM technique with sinusoidal reference.

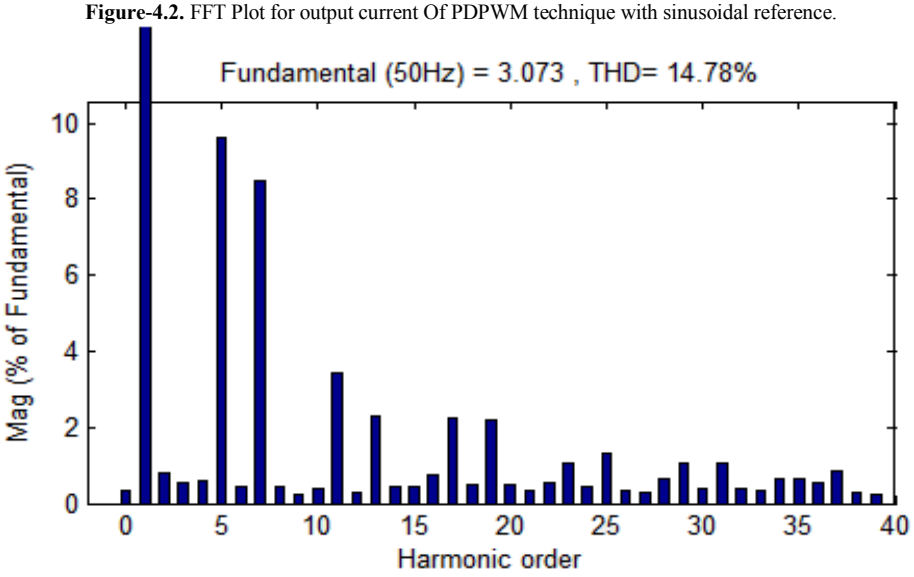


Figure-5. Three-phase output current waveform for PODPWM technique with sinusoidal reference

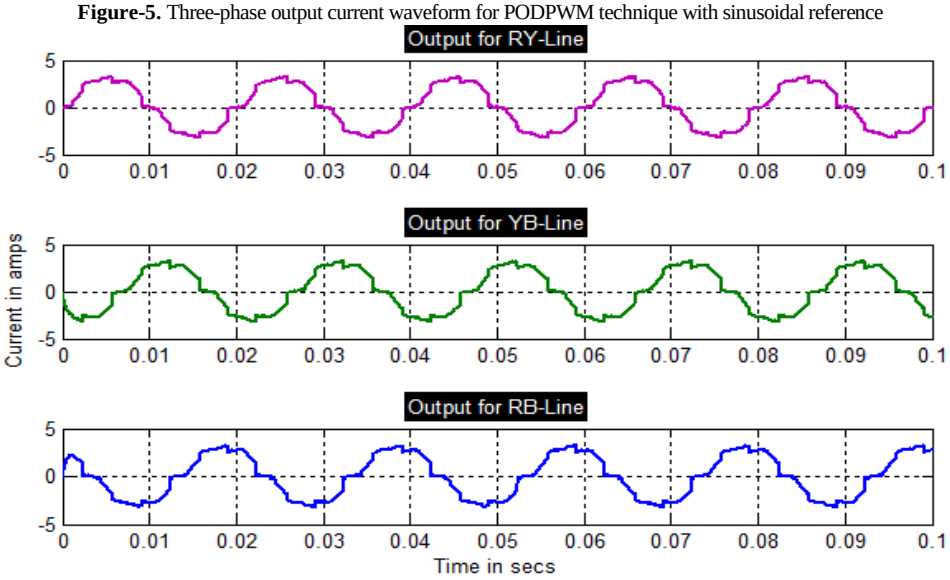


Figure-6. FFT Plot for output current of PODPWM technique with sinusoidal reference

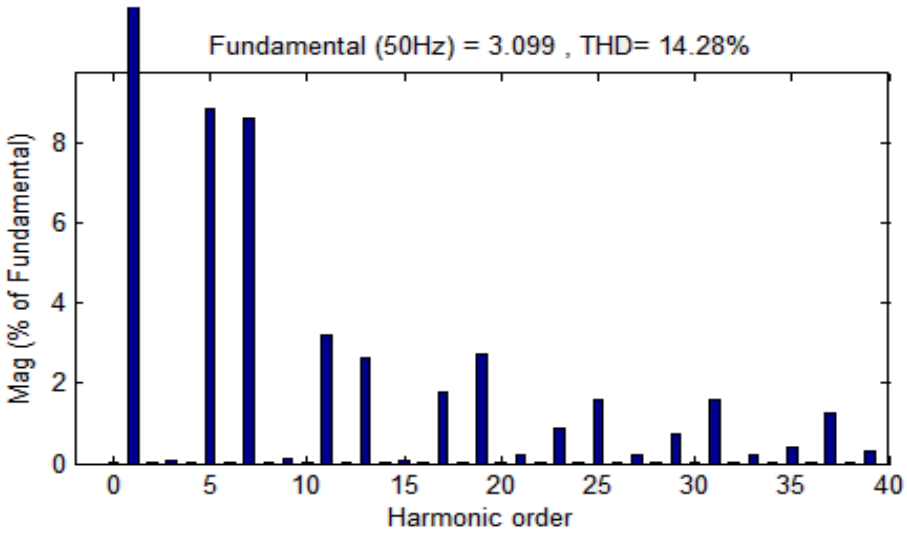


Figure-7. Three-phase output current waveform for APODPWM technique with Sinusoidal Reference

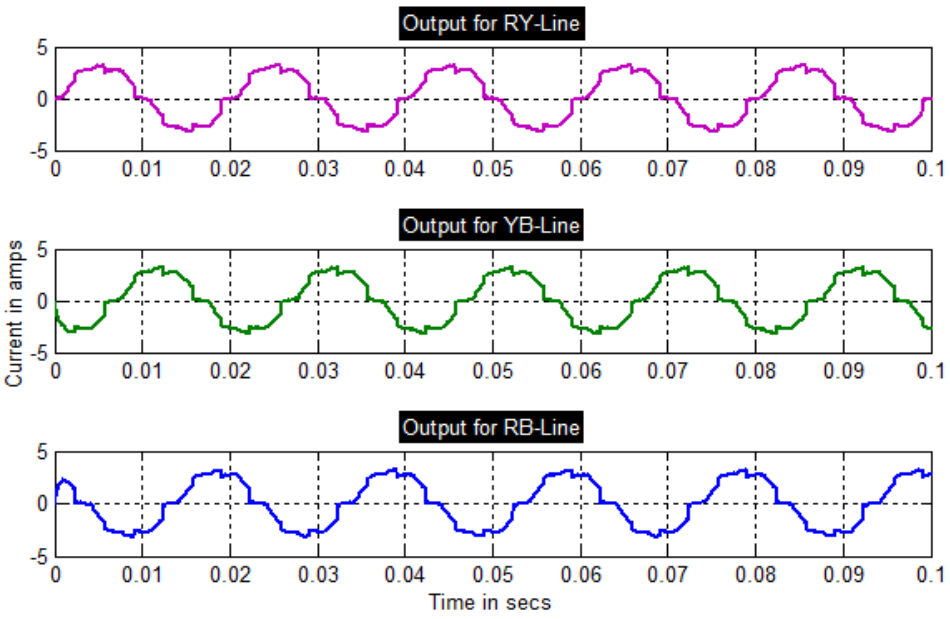


Figure-8. FFT plot for output current of APODPWM technique with sinusoidal reference.

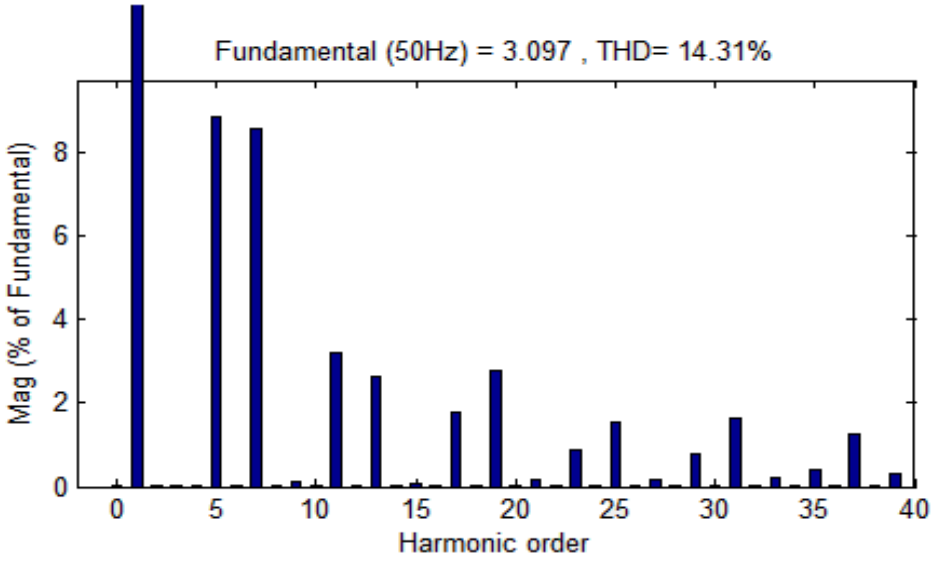


Figure-9. Three-phase output current waveform for COPWM technique with sinusoidal reference

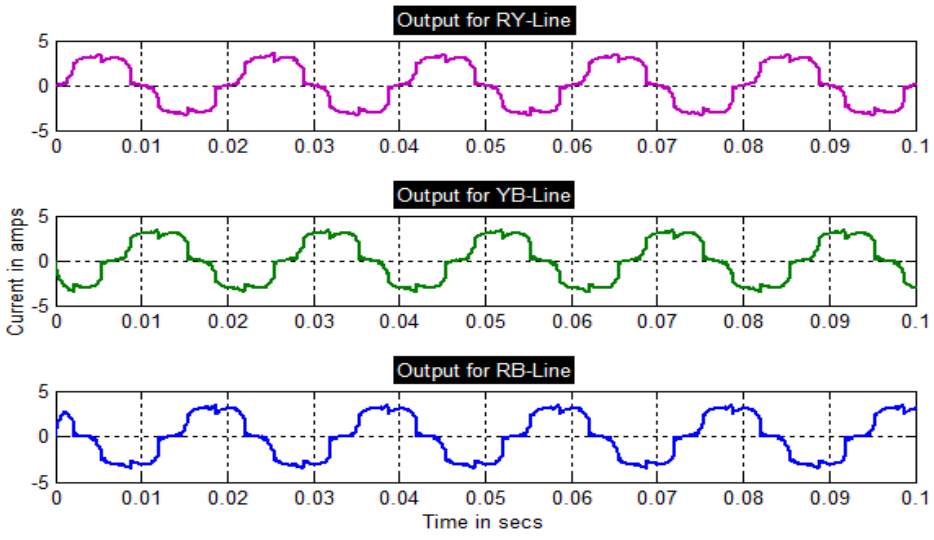


Figure-10. FFT plot for output current of COPWM technique with sinusoidal reference.

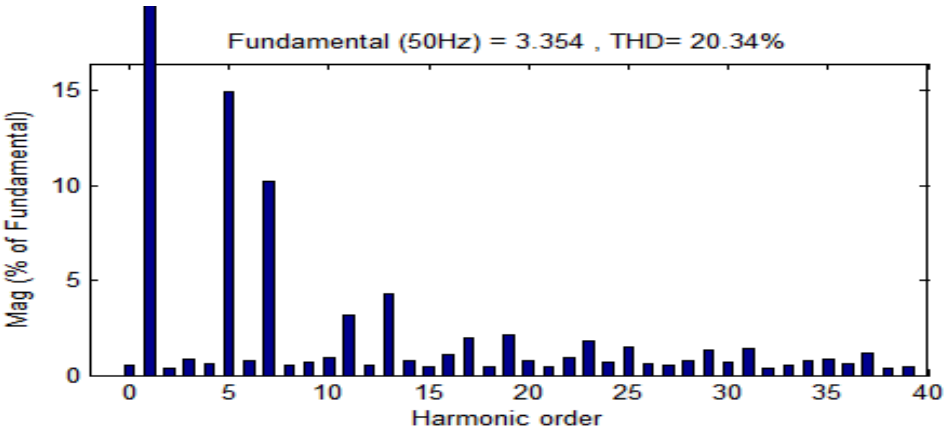


Figure-11. Three-phase output current waveform for VFPWM technique with sinusoidal reference

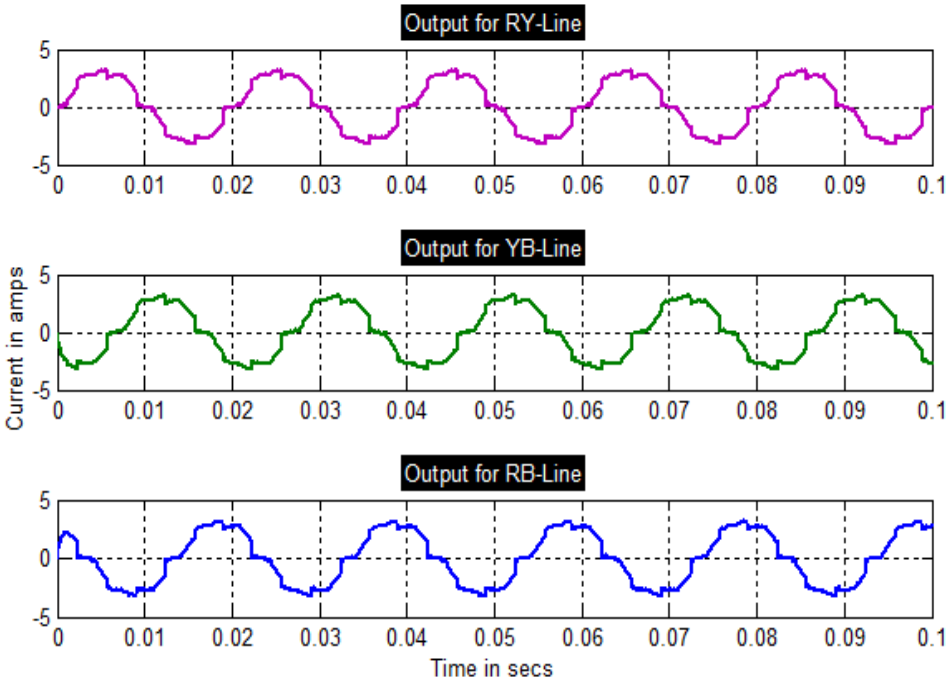


Figure-12. FFT plot for output current of VFPWM technique with sinusoidal reference

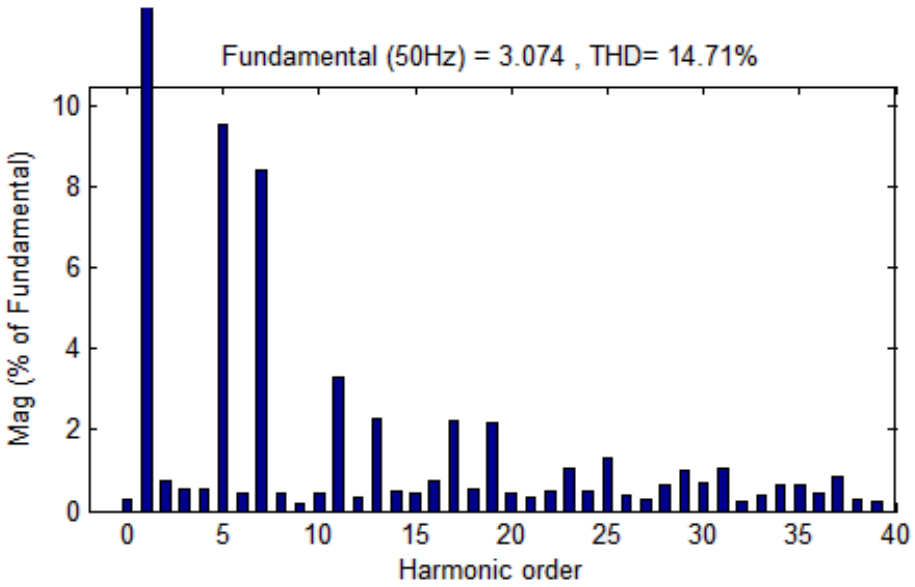


Figure 13 Three-phase output current waveform for PDPWM technique with trapezoidal reference

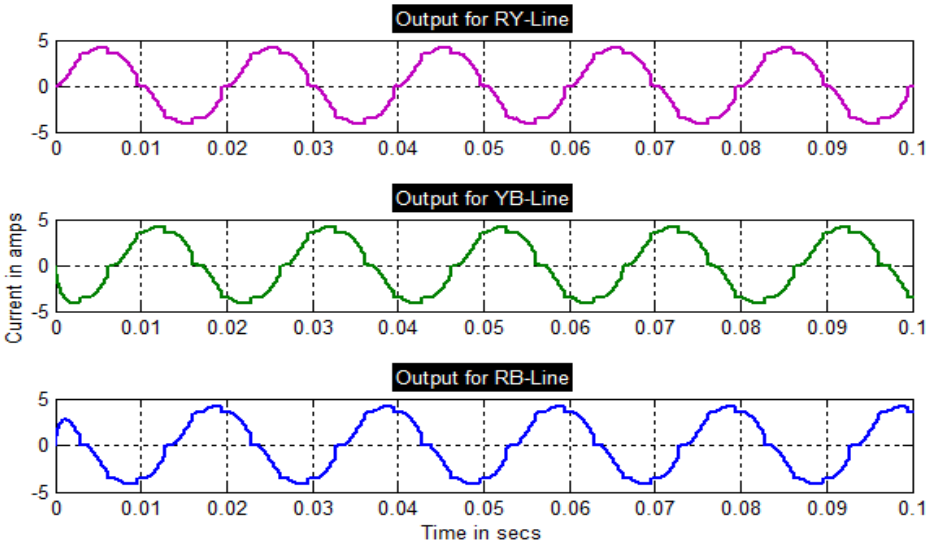


Figure-14. FFT plot for output current of PDPWM technique with trapezoidal reference

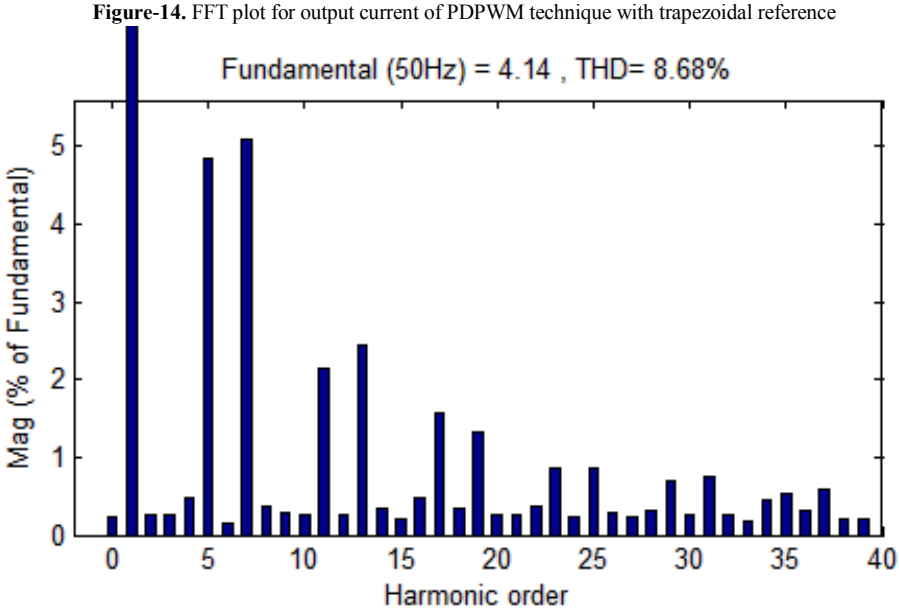


Figure-15. Three-phase output current waveform for PODPWM technique with trapezoidal reference

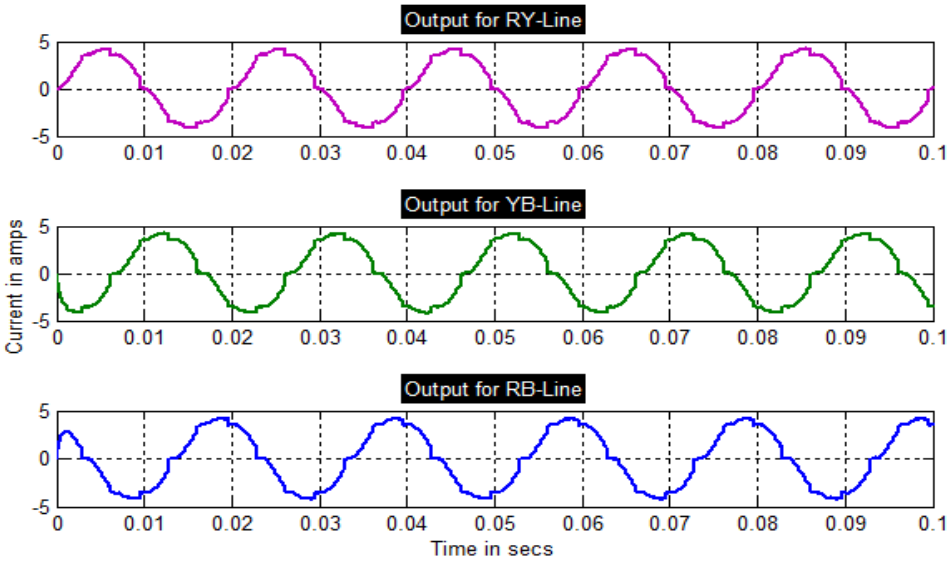


Figure-16. FFT plot for output current of PODPWM technique with trapezoidal reference

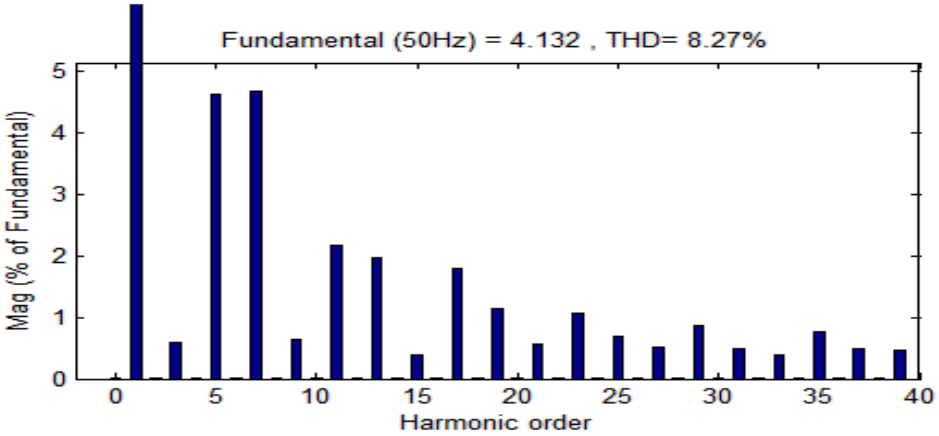


Figure-17. Three-phase output current waveform for APODPWM technique with trapezoidal reference

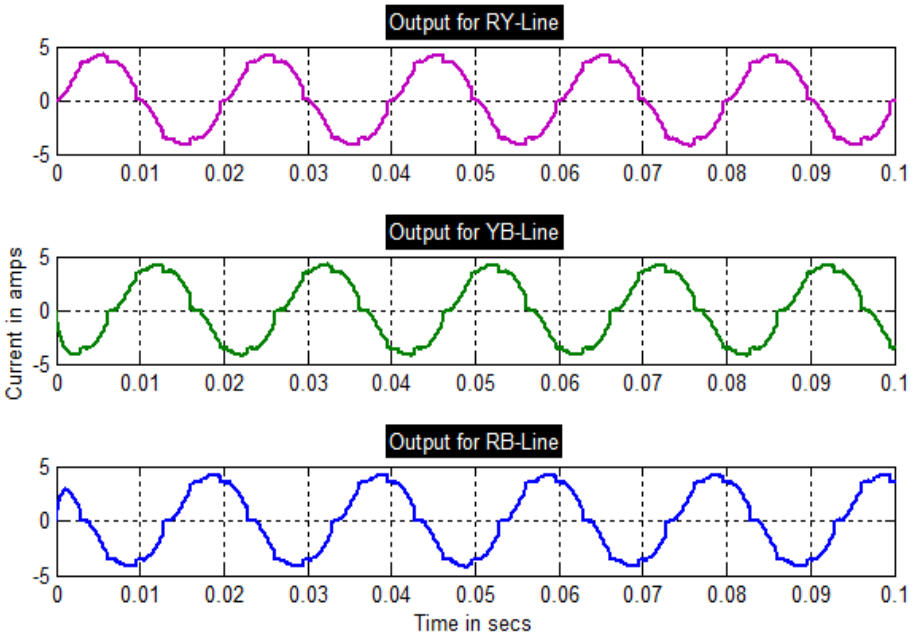


Figure-18. FFT plot for output current of APOD technique with trapezoidal reference

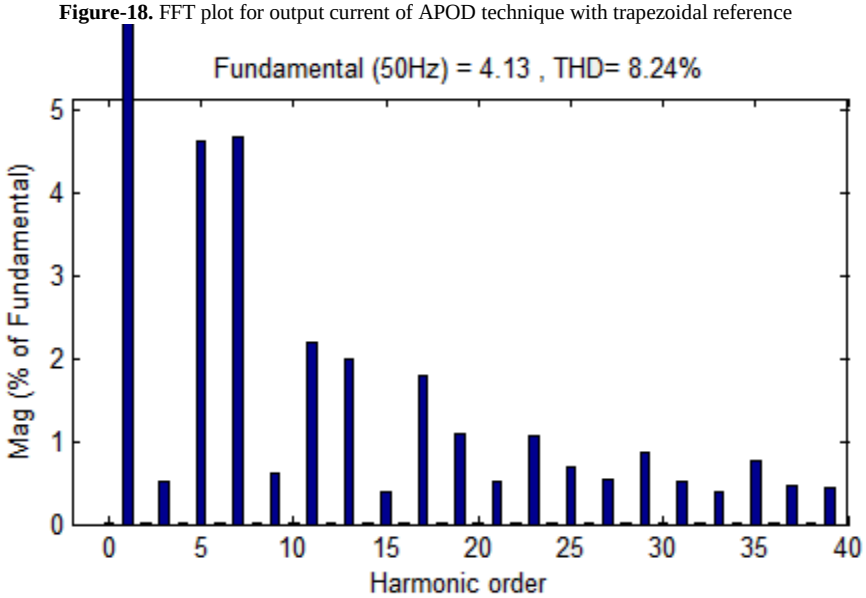


Figure-19. Three-phase output current waveform for COPWM technique with trapezoidal reference

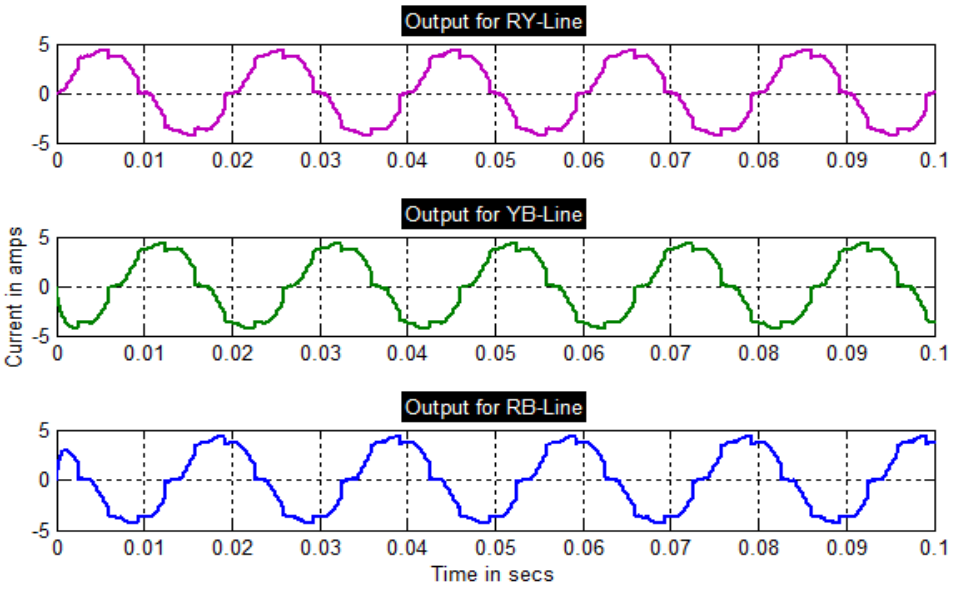


Figure-20. FFT plot for output current of COPWM technique with trapezoidal reference

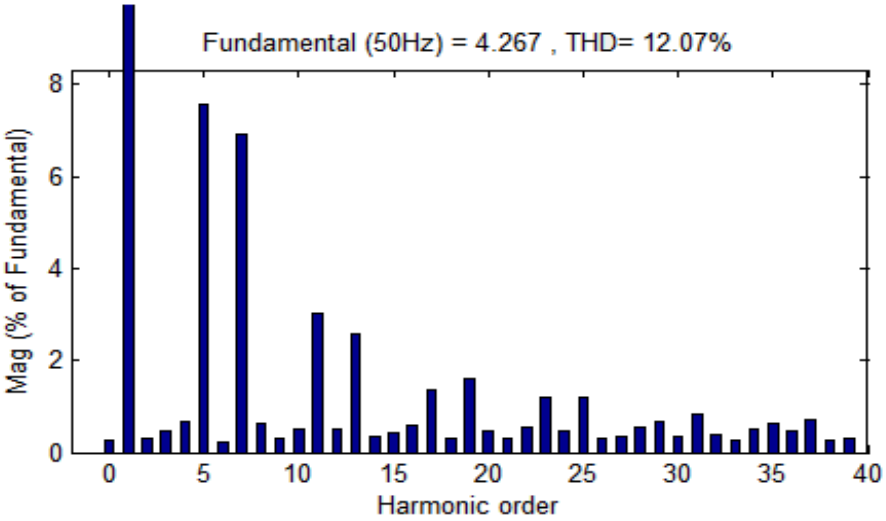


Figure-21. Three-phase output current waveform for VFPWM technique with trapezoidal reference

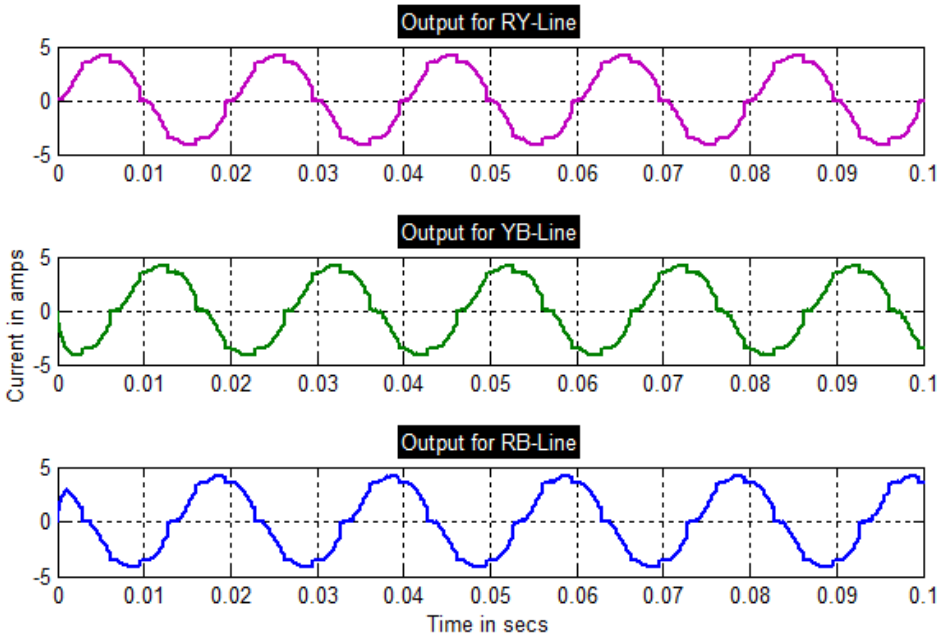


Figure-22. FFT plot for output current of VFPWM technique with trapezoidal reference

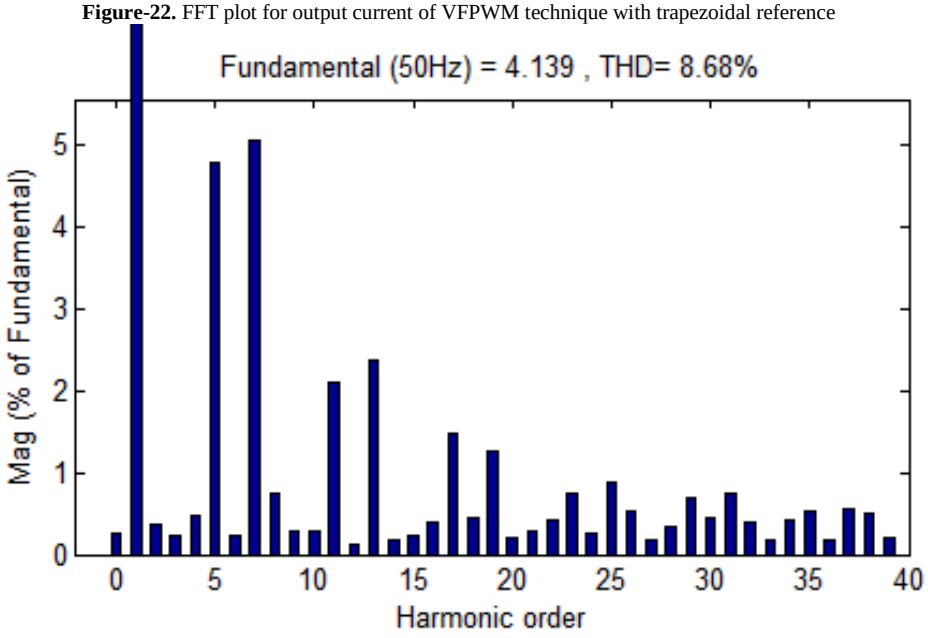


Table-2. %THD for different modulation indices with sinusoidal reference

m_a	PDPWM	PODPWM	APODPWM	COPWM	VFPWM
1	11	10.85	10.46	15.18	10.98
0.9	11.84	11.27	11.35	17.75	12.88
0.8	14.78	14.28	14.31	20.34	14.71
0.7	16.05	15.27	20.07	24.37	15.99
0.6	20.71	16.18	19.81	39.27	20.60

Table-3. I_{RMS} for different modulation indices with sinusoidal reference

m_a	PDPWM	PODPWM	APODPWM	COPWM	VFPWM
1	2.756	2.756	2.773	2.873	2.754
0.9	2.473	2.467	2.465	2.623	2.465
0.8	2.173	2.192	2.19	2.371	2.174
0.7	1.893	1.888	1.579	2.023	1.893
0.6	1.583	1.478	1.58	1.489	1.585

Table-4. I_{PEAK} for different modulation indices with sinusoidal reference

m_a	PDPWM	PODPWM	APODPWM	COPWM	VFPWM
1	3.897	3.897	3.921	4.063	3.895
0.9	3.497	3.489	3.487	3.709	3.486
0.8	3.073	3.099	3.097	3.354	3.074
0.7	2.676	2.67	2.233	2.861	2.677
0.6	2.239	2.237	2.234	2.106	2.241

Table-5. %THD for different modulation indices with trapezoidal reference

m_a	PDPWM	PODPWM	APODPWM	COPWM	VFPWM
1	8.08	7.68	7.67	11.19	8.12
0.95	8.34	8.10	8.12	11.68	8.32
0.9	8.68	8.27	8.24	12.07	8.68
0.85	8.77	8.28	8.28	13.63	8.78
0.8	9.78	10.18	10.17	14.14	9.74

Table-6. I_{RMS} for different modulation indices with trapezoidal reference

m_a	PDPWM	PODPWM	APODPWM	COPWM	VFPWM
1	3.256	3.271	3.268	3.218	3.239
0.95	3.083	3.086	3.084	3.113	3.083
0.9	2.928	2.922	2.921	3.017	2.927
0.85	2.765	2.759	2.754	2.886	2.765
0.8	2.592	2.584	2.585	2.79	2.595

Table-7. I_{PEAK} for different modulation indices with trapezoidal reference

m_a	PDPWM	PODPWM	APODPWM	COPWM	VFPWM
1	4.605	4.625	4.622	4.551	4.17
0.95	4.36	4.364	4.361	4.403	4.36
0.9	4.14	4.132	4.13	4.267	4.139
0.85	9.91	3.902	3.902	4.081	3.91
0.8	3.66	3.654	3.656	3.945	3.66

5. Conclusions

In this paper, a new basic unit for three phase symmetrical 9-level inverter with RL load is used. The nine level CMLI using seven switches is successfully introduced simulating the circuitry using MATLAB/SIMULINK and observed a clear stepped nine level waveform. It is found that the APODPWM dominates all other PWMs in the proposed configuration. The novel 9-level symmetrical inverter has lower THD compared to conventional symmetric topology.

References

[1] Al-Judi, A. and Nowicki, E., 2013. "Cascading of diode bypassed transistor-voltage-source units in multilevel inverters," *IET. Power Electron.*, vol. 6, pp. 554-560.

[2] Dordevic, O., Jones, M., and Levi, E., 2015. "Analytical formulas for phase voltage RMS squared and THD in PWM multiphase systems," *IEEE Trans. Power Electron.*, vol. 30, pp. 1645-1656.

[3] Fengjiang, W., Fan, F., Jiandong, D., and Bo, S., 2015. "Zero-Crossing disturbance elimination and spectrum analysis of single-carrier seven-level SPWM," *IEEE Trans. Ind. Electron.*, vol. 62, pp. 982-990.

[4] Ghazanfari, A., Mokhtari, H., and Firouzi, M., 2012. "Simple voltage balancing approach for CHB multilevel inverter considering low harmonic content based on a hybrid optimal modulation strategy," *IEEE Trans. Power Electron.*, vol. 27, pp. 2150-2158.

[5] Junfeng, L. K. W. E. C. and Yuanmao, Y., 2014. "A cascaded multilevel inverter based on switched-capacitor for high-frequency AC power distribution system," *IEEE Trans. Power Electron.*, vol. 29, pp. 4219-4230.

[6] Liming, L., Hui, L., Seon-Hwan, H., and Jang-Mok, K., 2013. "An energy-efficient motor drive with autonomous power regenerative control system based on cascaded multilevel inverters and segmented energy storage," *IEEE Tran. Ind Appli.*, vol. 49, pp. 178 – 188.

[7] Rahim, N. A., Chaniago, K., and Selvaraj, J., 2011. "Single-phase seven-level grid-connected inverter for photovoltaic system," *IEEE Trans. Ind. Electron.*, vol. 58, pp. 2435-2443.

[8] Ronny, G. d. A. C., Rene, P. T. B., Joao, A. F. N., and Grover, V. T. B., 2014. "Five-level t-type inverter based on multistate switching cell," *IEEE Trans. Ind. Appli.*, vol. 50, pp. 3857-3866.

[9] Samuel, P., Gupta, R., and Chandra, D., 2011. "Grid interface of wind power with large split- winding alternator using cascaded multilevel inverter," *IEEE Trans. Energy Conversion*, vol. 26, pp. 299-309.

[10] Yousedfpoor, N., Fathi, S. H., Farokhnia, N., and Abyaneh, H. A., 2012. "THD minimization applied directly on the line-to-line voltage of multilevel inverters," *IEEE Trans. Industrial Electron.*, vol. 59, pp. 373-380.